STATIC POWER

SMART | SOLID | SAFE

FUSED iSTS A, B & W

How does it work?

DETECTION

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The first step of the detection process involves attenuating the three waveforms we are interested in – supply 1, supply 2 and output supply – from 110V/240V_{AC} to 1V_{AC}. This provides the STS with the waveforms it requires at a reasonable level for analysis by the three Digital Signal Processors (DSPs).

We do this using an instrumentation amplifier attenuator configuration (no transformers). Each supply has its own DSP, where the AC waveforms are continuously sampled at 64 times per cycle and compared to real time maximum an minimum values.

If an error is detected (by say 3 consecutive 300µs samples above or below the limit) the DSP returns an output to the CPLD (which handles actions, explained below). While these "transient variations" are being monitored, the DSPs are also computing the three supplies RMS values and comparing them to an averaged value, where an output will be returned should any average value fall out of tolerance.

These processes are the same, though independent, for supply 1, supply 2 and supply 3.

For additional reliability, the supply 3 DSP provides redundant detection for supply 1 and supply 2, and also detects power loss at the output in case there is an internal failure.

ACTION

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Once a fault is identified, a Combinational Programmable Logic Device (CPLD) decides what actions to take and how to perform them.

The CPLD is a fast, simple and reliable hardware digital logic controller which uses combinational logic and a state machine to handle all the actions, sequences and timings required to safely and reliably transfer the connected critical load.

The program loaded on the CPLD is designed by in-house engineers specifically for use on the range of iSTS Static Transfer Switches. When the fault signals have been processed and the CPLD has decided what action to take, a signal is sent straight to the switching devices.

While the iSTS is capable of high level analysis of power supplies and intelligent interpretation of the results it acquires, its main function is still achieved through a simple twostep process – detect and act.

REPORTING and CONTROL

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The reporting, where necessary, is achieved by interrogating the "User Local LCD microprocessor". This is a separate, independent device and does not partake in any control function.

Information gathered by this microprocessor is organized and displayed on the front panel LCD. This information is also made available to the LAN WEB Server processor, providing Modbus, SNMP and HTTP which is again separate and plays no part in the operation of the STS, except to provide access for remote interrogation.

The simple display of state through the units bi-colour LED mimic is a more direct process, interfacing only with CPLD, (direct hardware lines)

Control pushbuttons, user relays and remote transfer inputs also interface directly with the CPLD, independently from the LCD or any microprocessors.

Control inputs can be seen to directly initiate an action in the case of user input, or influence an action in the case of fault input. More involved inputs, such as tolerance settings, are achieved through the LCD or LAN WEB server

PROTECTION - 1

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The power semiconductors used within the Static Transfer Switches are SCRs (Thyristors). They are very rugged and overrated (typically 4 to 6 times current capacity and 6 times voltage rating). Each source and neutral is protected by a 100A fuse.

These fuses ensure that the STS is safe, even when installed into distribution systems with extremely high fault currents. Even though the STS contains fuses, it is capable of very high overload and fault capability.

For safety reasons there needs to be some protection between the source and the load – the fuses are for final STS protection only. We would expect that the downstream fuses in the faulty equipment will clear first, thus loss of output due to internal STS failure is not likely to occur except for the most arduous operating conditions.

The STSs contain fuses that ensure safe installation for supply capacities up to 20kA.

The use of these fuses:

- Allows the STSs to be part of installations with extremely high fault current capability
- Allows currents of up to 100A for in excess of 30s and 200A for 25 cycles.
- Provides overload and fault withstand capacities of at least 2000% (400A) for 100ms without rupture of internal 100A fuse and without damage to the STS semiconductors.
- Provides fault current characteristics for safe and fast rupturing of fuses where fault current exceeds 2000A.
- At a fault current between 2kA and 20kA, the internal 100A fuse will rupture safely and the STS semiconductors will fail safely.

PROTECTION - 2

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The fault current values indicated above are seldom found in rack mounted arrangements as the cables interconnecting the source and the load limit the fault currents to very low values, below that which would cause the fuse to rupture. In reality, downstream protective devices are always smaller and operate well before the internal fuses operate near these levels.

In the rare event that one of the SCR/ Thyristors fail, the unit incorporates protection circuitry and reporting of SCR / Thyristor failures as Open Circuit or Short Circuit. Even when this occurs your load is fully protected – the functionality of the STS is impaired but not the continuity of power to the load.

In fact, there is no logic or process that disrupts power to the load. Events such as over-temperature, overcurrent and overload only raise an alarm. If unattended to a SCR/Thyristor failure may result but this does not result in loss of power to the load.

Current transformers on each source input continually monitor the currents. The output of the current transformers is used to display the loading for the STS and to undertake any overloading calculations to raise the appropriate alarm. In addition, a hardware peak value detector is used to detect load faults.

PROTECTION - 3

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In the case of a load fault the STS will not transfer to the other source which prevents the both sources being affected by the load fault.

There may be a loss of power to the connect equipment if the load fault condition has caused the active source to fail, however the source, for example a UPS, is usually able to transfer to its internal bypass and will have the extra capacity to clear the fault.

All other STSs (assuming there are others) will see the transient on the original source and safely transfer to the alternate source without affecting their connected loads.

It is possible although not recommended to isolate the load in case of a fault, but this is not a default operating condition. Our philosophy is to maintain power to the output of the STS not to disconnect it. Suffice it to say that either mode would be possible.

NO SINGLE POINT FAILURE - 1

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With all of this crucial control we have made sure that the failure of a component will not cause loss of supply to your

critical load. That's why we have implemented triple redundant power supplies one from each source and one from

the output. Any one is capable of maintaining the operation of the STS. A failure of any power supply will not cause the power bus to be affected because of the implementation of back-feed protection (diodes). the power bus (5 V_{DC}),

feeds multiple circuit elements (display, LAN, DSPs, front panel, CPLD, firing etc however, all of these have their own regulators and backfeed protection and current limiting to provide the 3.2V_{DC} and 1.8V_{DC} buses required to operate these blocks. Thus gain, any component that fails will not have an effect on any other block, will not have any effect on the operation and availability of power for the critical load., No matter where it occurs.

So this philosophy carries on throughout the STS implementation. The system has been designed not to drop the load even if this causes damage to the STS. So when the STS is overloaded we'll raise an alarm. Generous overload capability should provide sufficient time for the use to action reduction of load, however, if not responded to the SCRs will eventually fail, however, they fail in short, hence, power will be maintained the condition will be alarmed and the normal operation of transfer to the alternate source will be suspended until the STS is repaired and the SCR is replaced. But no power is lost. The thinking is that the cost of an SCR is always very much less than the cost to you losing your critical load.

NO SINGLE POINT FAILURE - 2

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The A1 and B1 units are naturally cooled, however the others have redundant fan configurations. If the fans were to fail or if the operating temperature/ environment was to rise (or even due to prolonged overloading), then eventually the SCRs will fail. Well before this we'll let you know of the over temperature condition by alarming and reporting, however, we will wait. We will not drop the load.

ENVIRONMENT

There is no de-rating for temperature and or altitude up to 3000m as all iSTS equipment has been qualified for full load operation to 65°C, unlike some manufacturers that limit operation to 30°C or below before de-rating. For practical reasons of maintaining reliability we prefer a maximum ambient temperature of 45°C with short term excursions up to 65°C without damage or deterioration. In the long term the more steady the operating temperature with an optimal of 20°C the longer the product life and the more reliable and the closer the MTBF is reached. That's

just the nature of electronics. Typically there is no wear-out, however, some electronic components do age.

Electrolytic capacitors (found in almost all electronic equipment), have a life time based on 000's of hours at a particular temperature and ripple. So there are different qualities of electrolytic capacitors some providing up to 10,000h at rated conditions, however, we don't use our capacitors at rated conditions. We can control the ripple current and the temperature so by calculation we can practically exceed 160,000h (18.2 years). We thus recommend a Preventative Maintenance Overhaul before 200,000h or sooner if the operating conditions are arduous.

POWER SUPPLY AND REDUNDANCY

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Each unit has a triple redundant power supply module. Only one power supply is required to operate the STS. Each of the power supplies has its source of AC power from a different source (Input Source 1, Input Source 3 and Output).

Each power supply has an extended operating range from $85V_{AC}$ to $305V_{AC}$ and are frequency insensitive.

A $5V_{DC}$ bus is generated from each of the sources, backfeed diodes are used to ensure that a failure of one power supply does not cause failure of any other power supply.

Each functionally separate logic functional block, for example DSPs, CPLD, Display, LAN and I/O, has its own set of linear regulators to provide a regulated, protected $3.3V_{DC}$ and $1.8V_{DC}$ power bus.

A failure of any functional logic block even if it was affecting its own power supply will not affect anything else and will not cause the STS to malfunction.

Protection against single points of failure such as this ensure that the STS is always in a safe state and able to continue to supply power to the output.

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